

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Joseph P. Abate, Registration No. 30,328; Jay H. Anderson, Registration No. 38,371; Ira D. Blecker, Registration No. 29,894; Steven Capella, Registration No. 33,086; Mark F. Chadurjian, Registration No. 30,739; James J. Cioffi, Registration No. 51,564; Harold H. Huberfeld, Registration No. 26,665; Todd M. C. Li, Registration No. 45,554; Anthony N. Magistrale, Registration No. 35,595; Margaret A. Pepper, Registration No. 45,008; H. Daniel Schnurmann, Registration No. 35,791; Tiffany L. Townsend, Registration No. 43,199; Steven J. Soucar, Registration No. 32,440; Eugene I. Shkurko, Registration No. 36,678; William P. Skladony, Registration No. 33,787; all of INTERNATIONAL BUSINESS MACHINES CORPORATION; and John E. Hoel, Registration No. 26,279; Christopher A. Hughes, Registration No. 26,914; Joseph C. Redmond, Jr., Registration No. 18,753; all of MORGAN & FINNEGAN, L.L.P.

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**Declaration and Power of Attorney for  
Patent Application**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

**STRUCTURE AND METHOD OF MAKING STRAINED CHANNEL  
CMOS TRANSISTORS HAVING LATTICE-MISMATCHED  
EPITAXIAL EXTENSION AND SOURCE AND DRAIN REGIONS**

the specification of which (check one)

☒

is attached hereto.

☐

was filed on \_\_\_\_\_ as Application Serial No. \_\_\_\_\_ and  
was amended on \_\_\_\_\_.

I hereby state that I have reviewed and understand the contents of the above- identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

NumberCountryDay/Month/YearPriority Claimed : N/A

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information material to the patentability of this application as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Applications:

Serial No.Filing Date Status: N/A